REMARKS

Applicants respectfully request reconsideration of the present application in view of the below remarks. Claims 13-22 are pending in the application. Claims 1-12 are withdrawn from consideration in the present application due to a restriction requirement. Claims 14-17 depend directly or indirectly from independent claim 13, and claims 19-22 depend directly or indirectly from independent claim 18.

I. FORMAL MATTERS

Drawings

Applicants note with appreciation Examiner's acceptance of drawings submitted on October 18, 2006.

Information Disclosure Statement submitted January 27, 2006

Applicants note with appreciation that the Examiner has initialed the references cited in the IDS Form SB08 submitted January 27, 2006, indicating that the considered references will be included on the face of any patent issuing from the present application.

II. REJECTIONS UNDER 35 U.S.C. §102(e)

Claims 13 - 17

The Examiner rejects claims 13 - 17 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,745,160 to Ashar et al. ("Ashar").

Applicants respectfully traverse this rejection at least because Ashar does not teach or suggest "a method of scheduling processing in a hardware threaded circuit, comprising: receiving inputs corresponding to unthreaded processing of an application; receiving information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined; and generating a hardware threaded schedule for processing the application with at least first and second one of

the processing elements being interconnected to enable dynamic resource sharing", as recited in claim 13.

The Examiner alleges that Ashar, at FIG. 15 and col. 4 line 8 to col. 6 line 11, teach "receiving inputs corresponding to unthreaded processing of an application." See Office Action at page 2. However, Applicant submits that Ashar does not describe this feature.

Ashar merely describes a verification methodology for scheduling of a circuit. The verification methodology appears to include verification of a schedule obtained from a behavioral description of a simulated circuit. Ashar describes the behavioral description as, for example, "a complete order on the operations executed *for each thread*" (see Ashar, col. 6 line 30 – 34, emphasis added). Applicants submit that "receiving inputs corresponding to *unthreaded* processing of an application," as recited in claim 13, is quite different from a verification of scheduling based on a behavioral description of operation executed for threads. Thus, Ashar does not describe "receiving inputs corresponding to unthreaded processing of an application", as recited in claim 13.

Furthermore, Examiner alleges that Ashar at FIG. 15 and col. 26, line 16 to col. 29, line 11 teaches "receiving information including processing dement (sic) resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined." See Office Action at page 2. Applicant submits that Ashar does not describe anything remotely resembling this claim feature. Rather, Ashar discloses "various behavioral descriptions that have been transformed through one or more of: introduction of cycle boundaries; operation reordering; loop unrolling winding; folding and pipelining; and through speculative execution of operation." See Ashar col. 26 line 25 – 29.

Applicants submit that verification of scheduling and handling of behavioral descriptions as described in Ashar is irrelevant to the receiving information step recited in claim 13. Further to this point, Ashar does not describe the *processing element resources* recited in claim 13; nor does Ashar describe a *number of processing elements*. Furthermore, Ashar does not describe receiving information for a *window size*. Even if Ashar did describe this feature, it does not

describe the window size as *corresponding to a number of downstream processing states to be examined.*

Accordingly, Applicant submits that Ashar does not describe "receiving information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined," as recited in claim 13.

In addition, Examiner alleges that Ashar at FIGS. 10 – 15, col. 26, line 30 to col. 30 line 48, and Summary section teach "generating a hardware threaded schedule for processing the application with at least first and second one of the processing elements being interconnected to enable dynamic resource sharing." Ashar does not describe this feature.

In the Summary section Asher describes an "uninterupted (sic) symbolic simulation procedure." (Ashar col.. 7, lines 42 – 43. The procedure "determine(s) whether, given the behavioral specification and the scheduled RTL, the outputs of the two descriptions correspond unconditionally to each other." (col. 7, at line 43 – 46). For example, Ashar further describes "checking correctness of transformations (between symbolic and behavioral descriptions) such as the movement of operations across conditionals." (col. 7, lines 59 – 62). The conditionals may include while loops and if-then statements.

FIGS. 10 – 13 of Asher appear to describe various scheduling case studies, including speculative scheduling (FIGS. 10a and 10b), communication protocols. (FIGS. 12a and 12b), and binary tree sort (FIGS. 13a and 13b). Further, FIGS. 14 and 15 appears to describe various embodiments of the verification methodology described in Ashar.

Applicants submit that the verification methodology described in Ashar is completely different from "generating a hardware threaded schedule for processing the application with at least first and second one of the processing elements being interconnected to enable dynamic resource sharing," as recited in claim 13. For example, FIG. 14 of Ashar appears to describe a loop invariants extractor, symbolic simulator, and equivalence prover.

FIG. 15 of Ashar appears to describe descriptions for schedule states and behavior states. The schedule and behavior states are converted to a schedule thread and a behavior thread, respectively, and an equivalence checker checks equivalence of the schedule states and behavior states. See Ashar FIG. 15, 15.6 and 15.7. In no way can Ashar be reasonably construed as describing generating a hardware threaded schedule, as claimed.

Furthermore, Ashar does not describe "generating a hardware threaded schedule for processing the application with *at least a first and second one of the processing elements*", as recited in claim 13.

In addition, claim 13 recites that the "at least first and second one of the processing elements are *interconnected* to enable resource sharing." Ashar clearly does not teach or suggest this limitation. Thus, Applicants submit that Ashar does not teach "generating a hardware threaded schedule for processing the application with at least first and second one of the processing elements being interconnected to enable dynamic resource sharing," as recited in claim 13.

In view of the above, Applicant submits that Claim 13 is patentably distinguishable over Asher. For at least the same reasons, Applicant submits that claims 14-22 are also distinguishable

Claims 18 - 22

The Examiner rejects claims 18 - 22, which are directed to a hardware threaded circuit system, under 35 U.S.C. §102(e) as being anticipated by Ashar. Applicants traverse this rejection at least because Ashar does not teach or suggest a task manager or "a plurality of processing elements coupled to the task manager, wherein first and second ones of the plurality of processing elements are interconnected for hardware threaded processing to enable dynamic borrowing of processing resources associated with the second one of the plurality of processing elements by the first one of the plurality of processing elements", as recited in claim 18.

The Examiner alleges that Ashar, at FIG. 15 and col. 12, line 43 to col. 13, line 33, describes a task manager. Applicant submits that Ashar does not describe anything that can be considered a task manager. Ashar appears to describe verifying a schedule of a circuit against a behavioral description of the circuit. See Ashar, col. 12, starting at line 43. Ashar describes *instructions* for enabling the computer to perform the *verifying*, the instructions comprising instructions for specifying the schedule, representing a behavior of the circuit, and selecting a schedule thread and corresponding behavior thread. Furthermore, the instructions appear to include checking equivalence. Applicant submits that the instructions in Asher for verifying a schedule of a circuit against a behavioral description of the circuit are completely different than the task manager recited in claim 18.

Moreover, Ashar does not teach "a plurality of processing elements coupled to the task manager, wherein first and second ones of the plurality of processing elements are interconnected for hardware threaded processing to enable dynamic borrowing of processing resources associated with the second one of the plurality of processing elements by the first one of the plurality of processing elements," as recited in claim 18. The Examiner alleges that Ashar, at FIGS. 10 – 15, col. 12, line 24 to col.., 16, line 68, and col. 26, line 30 to col. 30, line 48, describe this feature of claim 18. See Office Action at page 3. Ashar does not describe a plurality of processing elements coupled to the task manager because, as explained above, Ashar does not describe a task manager. Furthermore, Ashar does not describe that "first and second processing elements are *interconnected* to enable dynamic borrowing of processing resources," as claimed. Furthermore, Ashar does not describe "*dynamic borrowing of processing resources associated with the second one of the plurality of processing elements by the first one of the plurality of processing elements.*" See claim 18.

Thus, Applicants submit that Ashar does not teach a task manager or "a plurality of processing elements coupled to the task manager, wherein first and second ones of the plurality of processing elements are interconnected for hardware threaded processing to enable dynamic borrowing of processing resources associated with the second one of the plurality of processing elements by the first one of the plurality of processing elements", as recited in claim 18.

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Therefore, because Ashar does not teach all the elements of claim 18, Ashar does not anticipate claim 18, and the dependent claims there form, under 35 U.S.C. §102(e). Thus, Applicants respectfully request withdrawal of the rejections.

In view of the above, Applicants submit that pending claims 13 - 22 are in condition for allowance. Accordingly, a notice of allowance for these claims is respectfully requested.

The Examiner is respectfully invited to telephone the undersigning attorney if there are any questions regarding this Response or this application.

Applicant does not acquiesce to any assertion made by the Examiner not specifically addressed herein.

The Assistant Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 500845, including but not limited to, any charges for extensions of time under 37 C.F.R. §1.136.

Respectfully submitted,

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